

# Sequential Logic

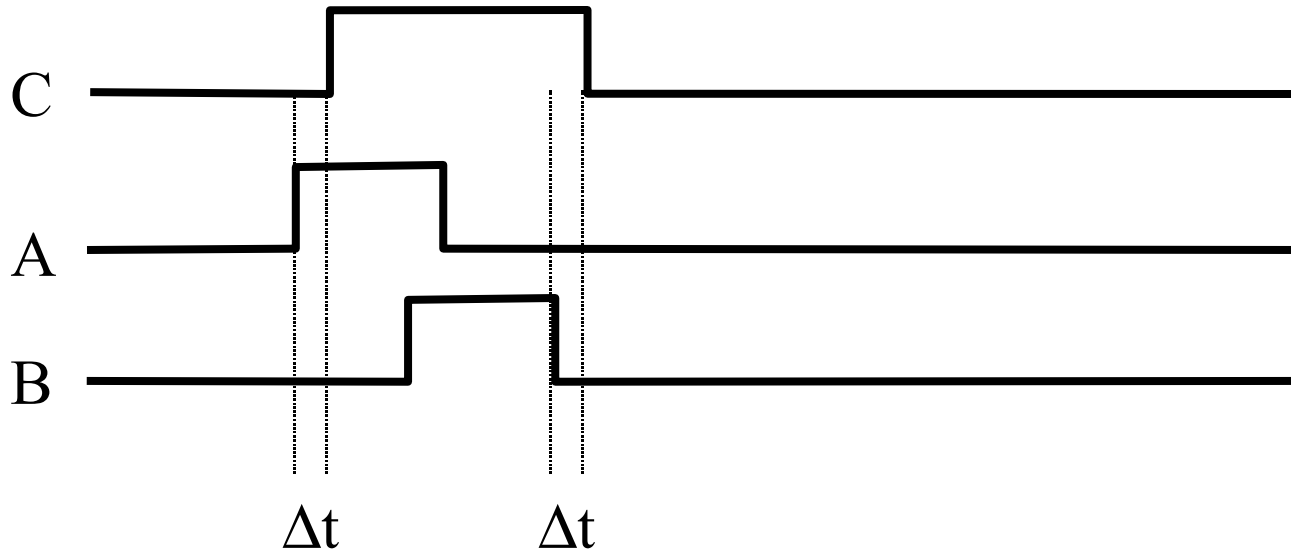
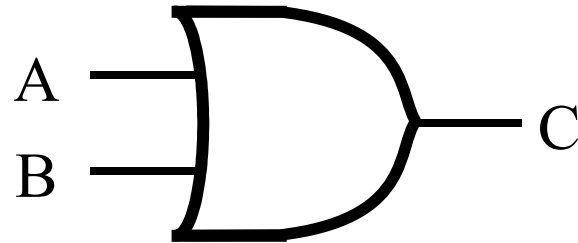
# Combinational vs. Sequential

- Combinational: output depends completely on the value of the inputs.
  - time doesn't matter.
- Sequential: output also depends on the *state a little while ago*.
  - can depend on the value of the output some time in the past.

# Memory

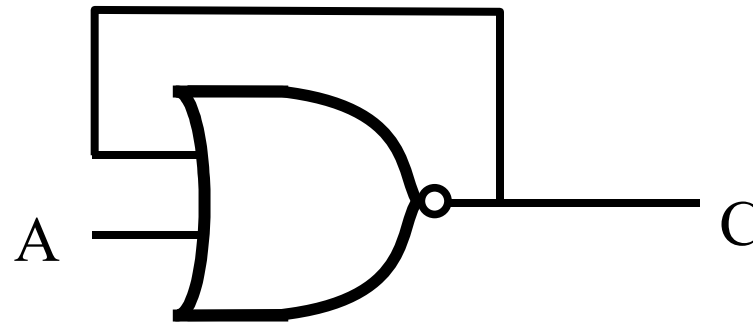
- Think about how you might design a combinational circuit that could be used as a single bit *memory*.
- Use your *memory* to recall that the output of a gate can change whenever the inputs change.

# Gate Timing



A	B	A nor B
0	0	1
0	1	0
1	0	0
1	1	0

# Feedback



What happens when A changes from 1 to 0?

- Try connecting the microphone input to the earphone output on your PC.
- Try holding a mirror in front of you while you are looking in a mirror.
- Try using [google.com](http://google.com) to search for the term “google”.

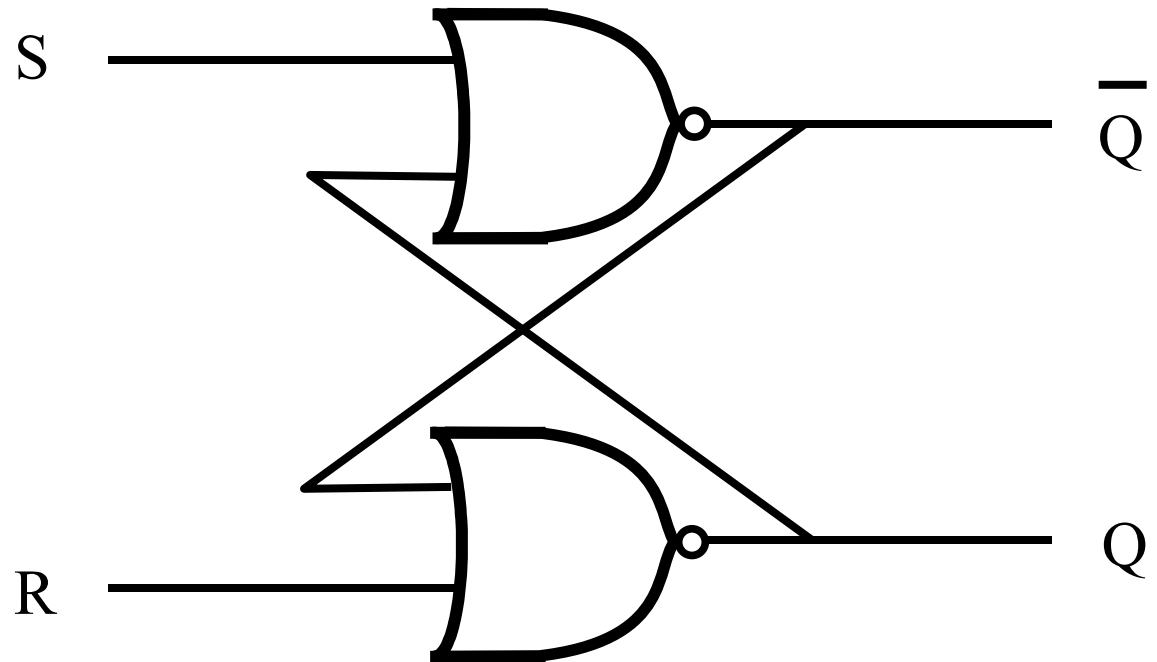
*Caution: the above experiments may result in opening a worm hole in your immediate surroundings!*

# Feedback can be stable

- It is possible to use feedback in a circuit that is predictable and *stable*.
- It is harder to tell what is going on (when compared to combinational circuits), but it is possible:
  - figure out what the output is at some initial time.
  - use that output to determine the next output.
  - continue until the worm hole contracts...

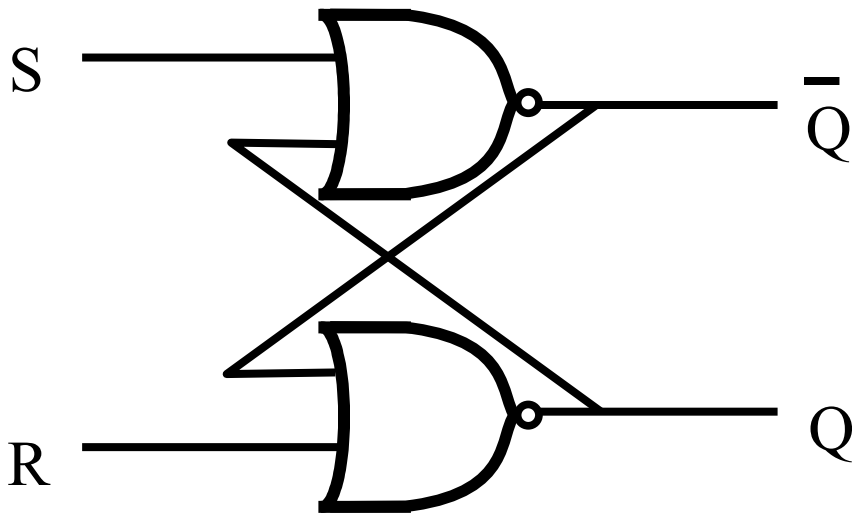
A	B	A nor B
0	0	1
0	1	0
1	0	0
1	1	0

## S-R latch



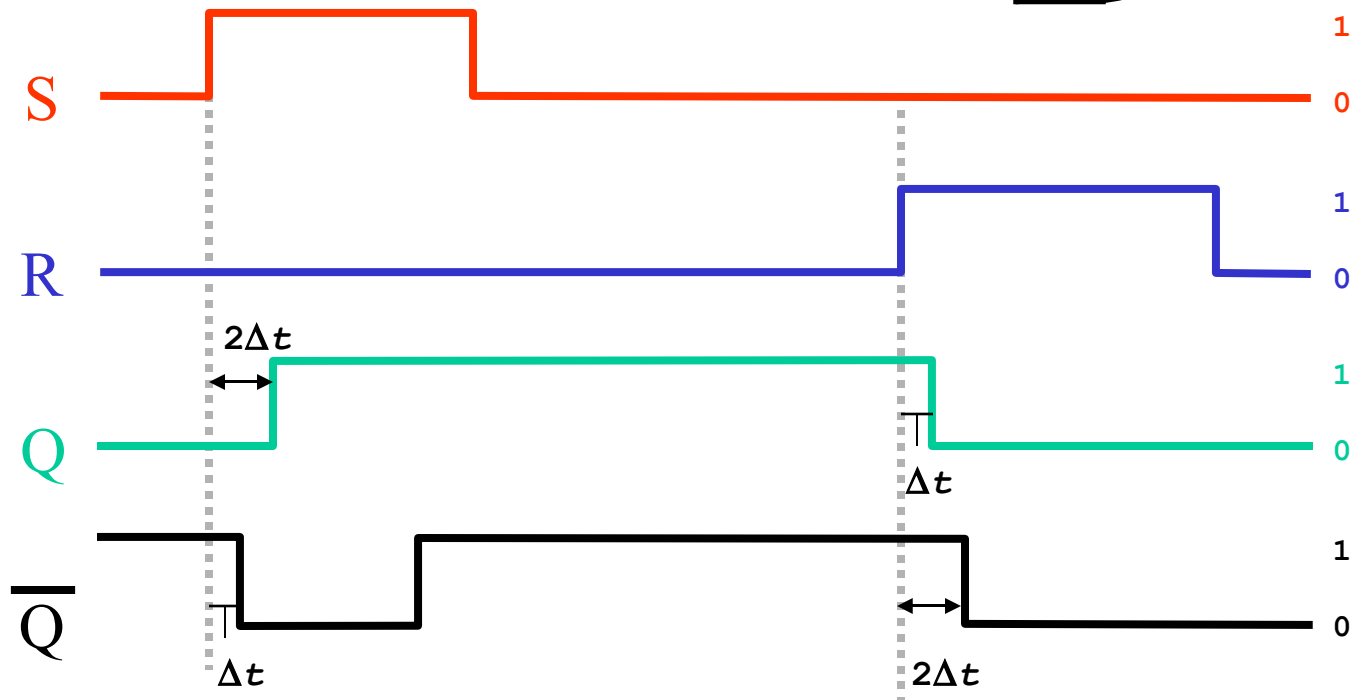
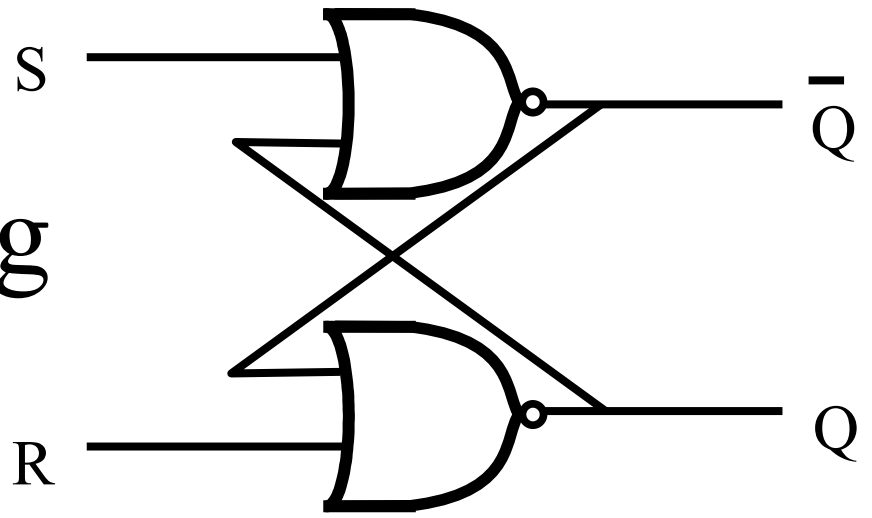
S stands for “Set” as in “Set to a 1”  
R stands for “Reset” (set to a 0).

# S-R latch Truth Table



$Q_t$	$S_t$	$R_t$	$Q_{t+1}$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	?
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	?

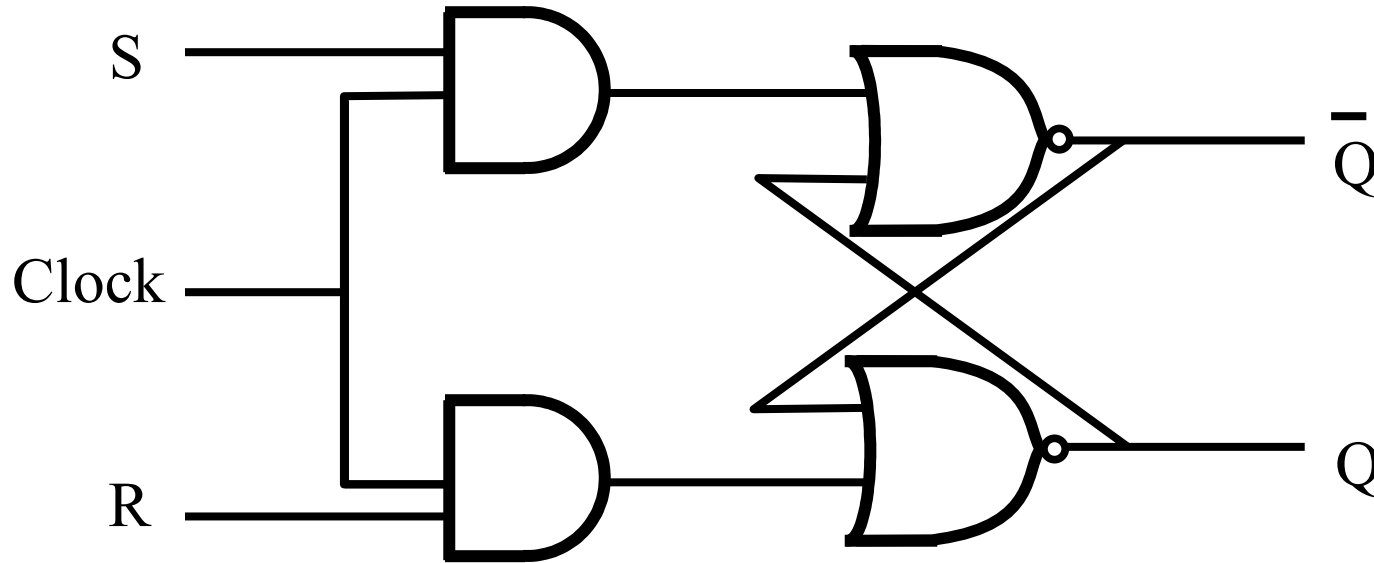
# S-R latch Timing



# Clocked S-R Latch

- Inside a computer we want the output of gates to change only at specific times.
- We can add some circuitry to make sure that changes occur only when a *clock* changes (when the clock changes from 0 to 1).

# Clocked S-R Latch

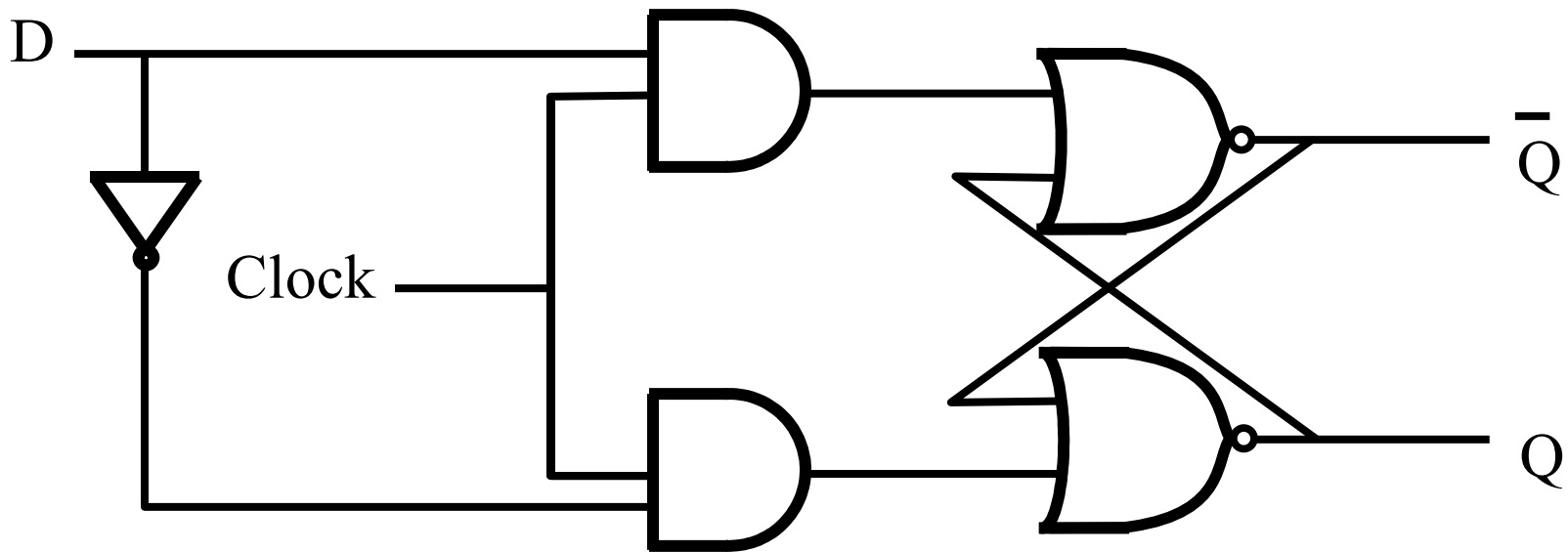


- Q only changes when the Clock is a 1.
- If Clock is 0, neither S or R *reach* the NOR gates.

# What if $S=R=1$ ?

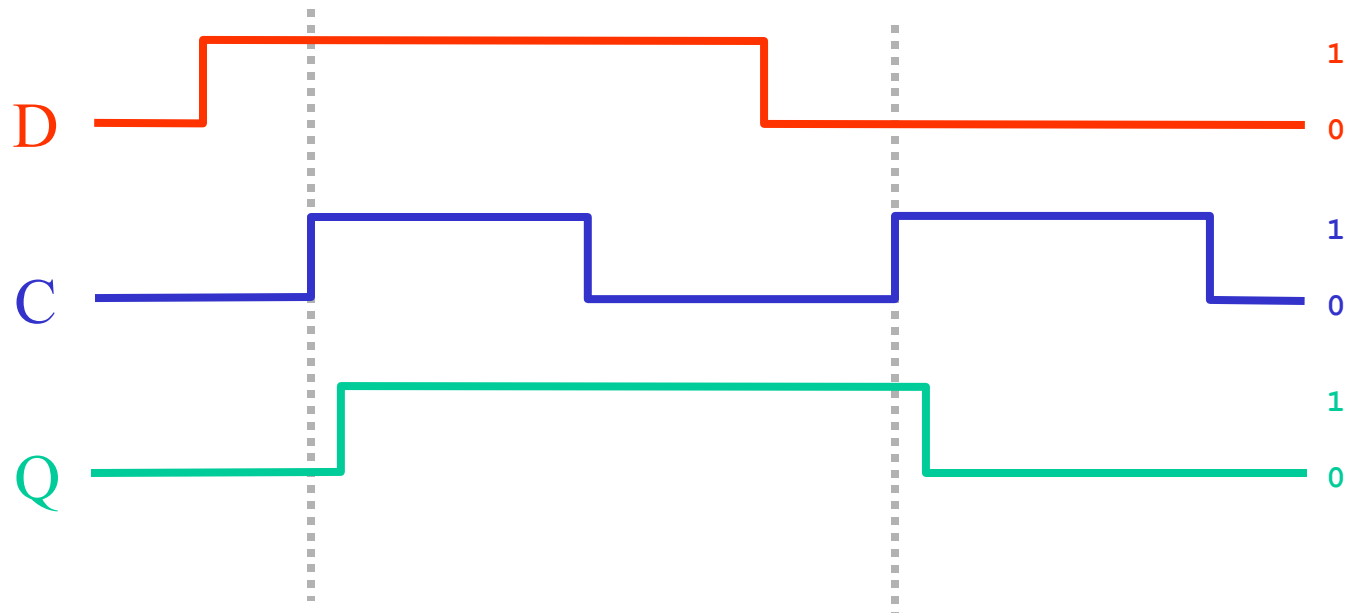
- The truth table shows “?” when  $S=R=1$ .
- The value of  $Q$  is undetermined.
  - The circuit is not *stable*.
- We can make sure that  $S=R=1$  now that we have a clock.

# Avoiding $S=R=1$ : D Flip-Flop



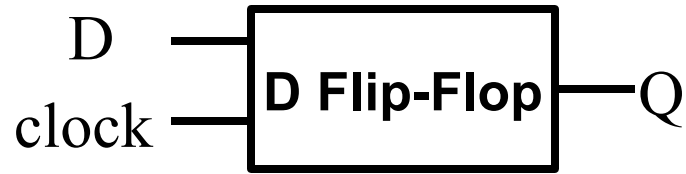


# D Flip-Flop Timing



# 8 Bit Memory

- We can use 8 D Flip-Flops to create an 8 bit memory.
- We have 8 inputs that we want to *store*, all are *written* at the same time.
  - all 8 flip-flops use the same clock.



# 8 Bit Memory

