

# Theodore C. Yapo

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- Experience**    **Cerberus Consulting, LLC, Andover Massachusetts**    September 2004 – Present  
*Founding Partner*
- Founded firm to provide consulting services in embedded systems. Implemented network-based video streaming systems for HD DVD production facilities. Created HD DVD player demonstration prototypes for trade show displays and field marketing. Developed embedded Linux systems, improving reliability and adding field upgradability for new HD DVD standard decoding devices.
- Cisco Systems, Boxborough, Massachusetts**    2002 – 2004  
*Engineering Manager, BEMRBU*  
*Program Manager uBR10k/PRE2*
- Responsible for delivery of next-generation forwarding engine for uBR10k Cable Modem Termination System. Defined required scope and functionality with marketing team. Lead 14-engineer team developing functional and detailed software design specifications, IOS C-code and network processor microcode. Planned and coordinated EDVT, RFDVT, MDVT, Development Test, Documentation, Customer Advocacy, and Manufacturing teams. Responsible for overall project planning and execution.
- Software Development Manager MC28U*
- Responsible for development of MC28U distributed architecture cable line card software. Managed software development team of 23 software engineers. Directed planning, execution and schedule for on-time delivery of product.
- Hammerhead Networks, Billerica, Massachusetts**    2000 – 2002  
*Principal Engineer*
- Hammerhead networks was a startup company building a second-generation parallel network processor based edge services router. Hammerhead was acquired by Cisco in June, 2002.
- Tools Team Lead*
- Lead team and developed simulation tools for Cisco PXF parallel network processor software development.
- Cycle Accurate Simulator - lead team developing RTL-derived simulator for 2x8 array network processor ASIC. Simulator was derived directly from Verilog RTL code to ensure cycle accuracy and correct behavior. Simulation environment allows use of in-line C code which gets executed concurrently with simulated microcode, allowing enhanced instrumentation and testing.
- System Simulator - lead team developing functional and RTL-derived cycle accurate system simulation of 64-CPU network processor array. System allows functional simulation in C or cycle-accurate microcode simulation. Included bridge to allow Cisco IOS control-plane code on production control-plane processor to interact with simulated data-plane microcode.

Memory Access Planner - developed graphical tool to plan microcode memory accesses to shared memory resources by 8 parallel CPUs. Tool allows planning for controller and memory conflict-free accesses resulting in deterministic system performance. Developed multi-platform dynamic HTML interface, using standard web browser to communicate with simulator. Code generated through planner achieves 97% of theoretical performance.

Microcode Tools Chain - lead team developing full suite of tools for microcode development and testing. Developed microcode source-level debugger integrated with emacs, unit test harness for microcode verification, coverage analysis tool, cycle annotation and stall detection tool, and microcode linter. Innovative tools chain enabled first router ping in 55 hours from arrival of prototype hardware.

#### *Microcode Lead*

Lead team developing network processor software for tunneling protocols and NetFlow flow-based accounting router functions using microcode tool chain. Features included MPLS, GRE, and IpinIP tunneling. Delivered functional and detailed design specifications, production microcode, and automated formal unit tests with 100% code coverage. Lead design, code, and unit test reviews.

**Oak Technology Imaging Group, Andover, Massachusetts**  
*Project Engineer*

1998 – 2000

iDSP Assembler - wrote high-level assembler for PM-441 parallel image processor in perl. Enhanced algebraic assembly language to allow memory allocation, variables with initializers, block scope for variables and register aliases, XML debugger interface, and modular re-use of component assembly routines. Assembler features HTML project browsing system, which automatically creates project documentation from high-level assembly code.

iDSP Debugger - designed novel 2-tier client-server DSP debugging architecture supporting DSP code development and chip design verification running on simulation, PCI development card, or target system. Implemented COM interface between debugger and multiple lower layers. Developed XML interface for accessing project debug information from assembler. Lead contractor implementing Visual Basic debugger front-end.

PM-44i SDK - created software development kit for PM-44i SIMD parallel-processing image processor DSP. SDK included system libraries for multi-tasking, inter-task communication, dynamic memory allocation, code and table compression, and messaging with system CPU. Libraries included PM-44i routines coded in assembly, and portable C routines to be called from embedded application firmware.

PM-44+ Demo Board - developed color copy image processing algorithms in parallel assembly for PM-44+ DSP demo board. Prototyped algorithms in C. Software provided full color copy functionality with board connected to off-the-shelf scanners and printers. Developed raster-to-swath conversion and printer driver running on DSP for “dumb” inkjet printing engines.

Base MFP Pipelines - developed re-usable base inkjet color/monochrome photocopy processing pipelines in PM-44i parallel DSP assembly language. Pipelines included code for linear filtering, color conversion, automatic text/image separation, halftoning, and printer formatting. Photocopied pages are segmented into text and image regions for optimal output processing. Text regions are thresholded and printed in black ink only, while image regions are halftoned using cyan, magenta, yellow and black inks. Developed FIR filters using Matlab to correct for scanner/printer responses. Base pipelines have been used in development of inkjet MFP products by several major printer/MFP manufacturers.

MFP Simulator - designed re-usable high-level interface to PCI DSP development cards. Designed flexible MFP (multi-function peripheral) embedded system simulator in C on top of interface for testing inkjet MFP DSP pipelines.

DSP Design Modeler - designed system for prototyping and simulating new parallel DSP chip architectures using C++. Chip designers use system to prototype core and chip designs. De-

veloped C++ class hierarchy allowing transparent implementation of synchronous processing elements. System allows rapid prototype design at register or functional level, or combinations of both.

ASIC Design Verification - lead microcode verification of PM-44i parallel image-processing DSP. Wrote assembly-language test suite to verify features of PM-44i DSP and test performance.

**SteelPoint Technologies, Boston, Massachusetts**

1996 – 1998

*Senior Consultant*

Responsible for the design, development and project management of custom software application development efforts.

Project Manager and Architect/Lead Developer for the City of Boston Inspectional Services Department Archival Image Storage System. This enterprise-wide client-server application allows for efficient search and retrieval of approximately 2.5 million imaged building permits for the 100,000 buildings within City. Designed and implemented search/list/detail paradigm search and retrieval application using PowerBuilder. Designed Microsoft SQL Server database using S-Designer; wrote stored procedures for efficient retrieval and maintenance of data. Created efficient programs and associated procedures for loading and indexing the large volumes of images and data into database and FileNet image storage system using Visual Basic.

Developed billing system for fixed-income financial management firm. Performed analysis of existing business procedures, and created client-server solution for their automation, including calculation-intensive performance-based analytics. Designed and developed system including Informix stored procedures using a PowerBuilder front-end. Integrated new billing system with legacy portfolio management system.

Developed fund performance calculation/analysis system as part of a large portfolio management system. Devised efficient database structures and algorithms for use with time-series performance data. Made extensive use of Microsoft SQL Server stored procedures for calculating performance numbers, blending custom benchmarks and facilitating on-line analysis.

**Wellington Management Company, Boston, Massachusetts**

1994 – 1996

*Assistant Vice President*

Managed team of 5 developers and technical specialists supporting international equities department. Responsible for day-to-day system operations, migration from legacy mainframe systems to client-server applications. The team supported an end user community of 40 Portfolio Managers, Financial Analysts, and Administrative Staff. The position included substantial end-user contact to identify and clarify needs, perform analyses of business processes, and design systems to automate, streamline and assist the end user in their tasks.

*Developer* Developed international equities competitive portfolio analysis model in Mathematica. System uses statistical models to estimate competing portfolio product's asset allocations. Developed multi-currency performance system written in C/embedded SQL communicating with an Interbase database server. Ported the code to HP Allbase back-end. Developed Visual Basic application for caching financial data collected from data services. System allowed users to download data to local Access database automatically as part of nightly batch processing. Locally cached data could then be accessed quickly for performing interactive analysis. Created Microsoft Excel add-in for data gathering from HP3000 databases. System exposed Excel worksheet functions for gathering various time-series information stored in mainframe databases. Users are able to interactively create worksheets which can update themselves automatically as data changes, or at the users' discretion. Designed and implemented system for automatic creation of end-users' Excel spreadsheet models from legacy system databases. Included creation of portable C-program to write Excel binary files on multiple platforms, and scripting for automatic distribution of nightly production data to users' file servers.

**Atlantic Aerospace Electronics Corp., Waltham, Massachusetts** 1993 - 1994  
*Member, Technical Staff*

Responsible for algorithm design, implementation, and testing.

Open-pit mine detection - developed algorithm for recognition of open pit mining sites from multispectral (SPOT) satellite imagery. System detects and classifies mines using a number of features extracted from image data. Enhanced algorithm for multi-sensor fusion to enhance imagery by combining high-resolution panchromatic images with lower-resolution multi-spectral images. Converted Matlab prototype to C module for PCI remote-sensing package.

Fascimile enhancement - developed algorithms for enhancement of intercepted fascimile transmissions using morphological operations. Created system for fast (10-20x improvement) binary morphological image processing, using pixels packed into long integers in C. Implemented system in portable C-code for multiple platforms. Image operations (morphological erosion/dilation, region labeling and counting, and others) are performed on images stored in packed format, providing dramatic speed and memory usage improvements. Produced object-oriented, multi-data type image processing toolbox, written in C.

**Rensselaer Polytechnic Institute, Troy, NY** 1992 - 1993  
*Teaching Assistant*

“Laboratory Introduction to Embedded Control” - laboratory course in embedded control using HC6811 microcontroller programmed in C. Lab duties included helping students debug embedded code.

**Education** **M.S., Engineering Physics** May 1994

Rensselaer Polytechnic Institute, Troy, NY.

Thesis: Developed an algorithm for compressing images to 0.2-0.7 bits/pixel using an adaptive quadtree-structured mesh model and an efficient sparse-system solver. Produced software toolbox package using the algorithms, implemented in C.

**B.S., Engineering Physics** May 1992

Rensselaer Polytechnic Institute, Troy, NY.

**Publications** “Neural Vector Quantization for Image Compression” M.J. Embrechts and T.C. Yapo, Presented at ANNIE '93, St. Louis, Missouri, November 1993.

“Prediction of Critical Heat Fluxes using a Hybrid Kohonen-Backpropagation Neural Network” T.C. Yapo, M.J. Embrechts, S.T. Cathey, and R.T. Lahey, Jr in *Intelligent Engineering Systems Through Artificial Neural Networks*, Vol II ASME Press, 1992.

“The Application of Neural Networks to Two-Phase Flow Regime Identification” M.J. Embrechts, R.T. Lahey, Jr, and T.C. Yapo in in *Intelligent Engineering Systems Through Artificial Neural Networks*, Vol II ASME Press, 1992.